AFT 34 AMDT

WHAT IS CLAIMED IS

~~Patent Claims:~~

1. An integrated circuit of reduced parasitic capacitive influences comprising an insulating layer (7) buried in the semiconductor substrate (8), characterized by the insulating layer (7) being at least 5 µm thick and is locally restricted to specific areas of the integrated circuit, i.e. to specific passive elements.

2. ~~Integrated~~ circuit according to claim 1, characterized by the fact that the partial insulating layer (7) of a thickness of at least 5 µm locally restricted to the area of one or more integrated inductances, one or more integrated resistors, one or more integrated capacitors, one or more integrated bonding pads and/or one or more conductors and buried in the semiconductor substrate (8).

3. ~~Integrated~~ circuit according to claim 2, characterized by the fact that the integrated inductance consists of at least one upper metal plane (1) for realizing a spiral, and insulating layer (2), a lower metal plane (3) for forming a contact of the inner connector (10), an insulating layer (4), a field oxide layer (5), a channel stop layer (6), a buried local insulating layer (7) of a thickness of at least 5 µm as well as a semiconductor substrate (8).

4. ~~A~~ Method of fabricating an integrated circuit by means of CMOS or CMOS compatible silicon technologies with local buried insulation, comprising ~~characterized by~~ the method steps

- masking of the surface of the silicon wafer,
- forming moats of a depth of at least 5 µm and ribs in a width ratio of about 3.2 as well as a moat wider by about 25 % drawn around the entire array of moats and ribs, by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs

followed by oxide removal for precisely optimizing the ratio between the widths of the ribs and the moats for the purpose of reducing prestresses and possible formation of displacement in the successive process step,

- total oxidation of the ribs to silicon oxide and at least filling of the remaining moats adjacent to the surfaces by precipitating silicon dioxide, whereby cavities remain in the middle area of the oxide area which offer the additional advantage of an effectively increased dielectric constant,
- CMOS process or CMOS-compatible silicon process for the fabrication of the individual elements of the integrated circuit by utilization of the partial steps inherent in the given process for fabricating the elements of the integrated circuit, passive elements of the integrated circuit being formed for the purpose of reduced parasitic influences directly above the area of the buried insulation layer (7) of at least 5 µm thickness.

5. The method ~~Method~~ according to claim 4, further comprising ~~characterized by~~ the process steps of

- masking of the surface of the silicon wafer,
- forming moats at least 5 Mm deep and ribs by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs followed by oxide removal for optimizing the ratio between the widths of the ribs and the moats,
- total oxidation of the ribs to silicon oxide and at least filling of the moats adjacent to the surfaces by precipitating silicon dioxide,
- CMOS process or CMOS-compatible silicon process for the fabrication of an inductance above the area of the buried thick oxide using the contact and conductor system present in the given process.

6. The method ~~Method~~ according to claim 4 ~~or 5, characterized by~~ further comprising the step of etching moats of a depth of at least 5 µm, the width of the ribs and moats being selected such that during a subsequent complete transformation of the ribs into silicon

dioxide by oxidation the moats are closed but for a residual width of about 100 nm to 300 nm.

7. The ~~M~~ method according to claim ~~one or more of claims~~ 4 ~~to 6, characterized by the fact that~~ wherein moats of at least 5 µm depth are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2 µm are formed and that this array of moats and ribs is surrounded by a wider moat of a width of about 1.5 µm.

8. The ~~M~~ method according to claim ~~one or more of claims~~ 4 ~~to 6, characterized by the fact that~~ wherein the moats of a depth of at least 5 µm are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2. µm are subsequently formed by an additional sacrificial oxidation step.

Add B1